REMARKS

Claims 1-16 are pending in this application, of which Applicants amend claims 1, 3, and 8.

Claim Amendments

Applicants amend claims 1, 3, and 8 to more appropriately define the claimed subject matter. These amendments are supported at, for example, page 14, lines 20-24, of the Specification of the instant application as originally filed.

§112, Second Paragraph, Rejection of Claims 1-16

The Examiner rejected claims 1-16 under 35 U.S.C. § 112, second paragraph, because the term "test vectors that pass through the changed logic cones" in claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 is allegedly vague and indefinite. Claims 1, 3, 5, 8, 9, 12, 13, 15, and 16 were amended to recite "test vectors that activate the changed logic cones" in the Amendment filed on February 1, 2006, and entered concurrently with a Request for Continued Examination. Thus, claims 1, 3, 5, 8, 9, 12, 13, 15, and 16, and claims 2, 4, 6, 7, 10, 11, and 14 that depend therefrom, should be allowed over § 112, second paragraph.

§102(b) Rejection of Claims 1-16 over Gilbert et al.

The Examiner rejected claims 1-16 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,805,861 to Gilbert et al. ("*Gilbert et al.*"). Applicants respectfully traverse the rejection for the following reasons.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102, each and every element of the claim at issue must be found in the reference, either

expressly described or under principles of inherency. Furthermore, "the elements must be arranged as required by the claim." M.P.E.P. § 2131. See also *Richardson v. Suzuki Motor Co., Ltd.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989).

Claim 1

Gilbert et al. fails to anticipate claim 1 for at least the reason that *Gilbert et al.* does not disclose a circuit designing apparatus comprising, inter alia, "**a logic verification unit**[;] **a profile information generating unit configured to detect information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification, for each test vector, and to generate a profile information relating the test vector to the logic cones activated by the test vector**[; and] **a test vector classifying unit configured to classify the test vectors into test vectors that activate the changed logic cones and test vectors that do not activate the changed logic cones, by searching for the test vectors related to the changed logic cones in the profile information, wherein the logic verification unit inputs the test vectors that activate the changed logic cones into the changed circuit description, compares an output signal of the changed circuit description with an expected value of the output signal, and judges the validity of the changed circuit description in accordance with a result of the comparison**," as recited in amended claim 1.

Instead, *Gilbert et al.* discloses "[a] method used by an electronic design automation system for stabilizing the names of components and nets of an integrated circuit from one design version to another" (Abstract). A Cone Graph Compare (CGC) module reads an old design and a new design from a Logic Design Database. "The

CGC module then corrects the component and net names ... by analyzing the cones of logic contained in the design, comparing the old and new designs and assigning new names as needed. ... [T]he CGC module writes the name corrected design into the Logic Design Database" (Col. 11, line 62 to Col. 12, line 9).

In reference to claim 1, the Examiner alleges that the "user-defined names" (disclosed at Col. 11, lines 55-61) and "new names" (disclosed at Col. 12, line 28) of *Gilbert et al.* constitute the recited "test vectors" (Office Action of 11/04/05, pp. 3-4).

However, a "test vector" is an assignment of values to input variables of the circuit description to simulate the circuit that is described by the circuit description. One of ordinary skill in the art would not consider a "name" to constitute such a "test vector." For example, neither the "user-defined names" nor the "new names" of *Gilbert et al.* constitute "test vectors" that are inputted to a circuit description for a logic verification and "activate logic cones." The "names" are also not inputted "into the changed circuit description" such that a logic verification unit "compares an output signal of the changed circuit description with an expected value of the output signal, and judges the validity of the changed circuit description in accordance with a result of the comparison," as required by claim 1. Thus, the "user-defined names" and "new names" of *Gilbert et al.* do not constitute the "test vectors" as recited in claim 1.

Since *Gilbert et al.* fails to teach each and every element of claim 1 in the portion cited by the Examiner or any other portion, claim 1 and claims 2 and 12-14 that depend therefrom are not anticipated by *Gilbert et al.* Applicants request the Examiner to withdraw the rejection of claims 1, 2, and 12-14 under § 102(b).

Claims 3-11, 15, and 16

Claims 3 and 8, although different in scope from claim 1 and from each other, recite elements similar to those discussed above with respect to claim 1. Claims 3 and 8, and claims 4-7, 9-11, 15, and 16 that depend therefrom, are therefore allowable over *Gilbert et al.* for at least the reasons set forth above.

CONCLUSION

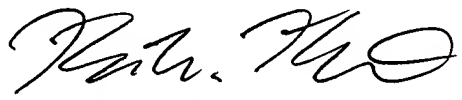
In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 4, 2006

By: 

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